XNOR Gate Design Using Static CMOS Logic

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##### **Abstract**

XNOR gate is an important logic gate in digital electronics. It is used in error detection circuit as even or odd parity checker and encoding operation in digital communication. It is also used for bit manipulations in ALU. The static CMOS logic comprises of pull-up network (PUN) and pull-down network (PDN) are used to design any digital logic circuit in CMOS. This paper presents the design of XNOR gate using static CMOS logic.

# **Reference Circuit Details**

Exclusive-NOR gate (XNOR) output will be high when, even number of its inputs are high or all the inputs are low, else output will be low for other cases. The truth table for two input XNOR gate is given below.

|  |  |  |
| --- | --- | --- |
| Input | | Output |
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Table 1 XNOR Gate Truth Table

In static CMOS logic pull-up network consists of pmos and pull-down network consists of nmos. Depending upon which network is activated, it drives the output to high or low respectively. Boolean equation for XNOR gate is given below.

Since static CMOS logic produce active low, double complement the above equation and simplify the equation using De Morgan’s theorem.

This equation is used to design the circuit.

# **Reference Circuit Design**

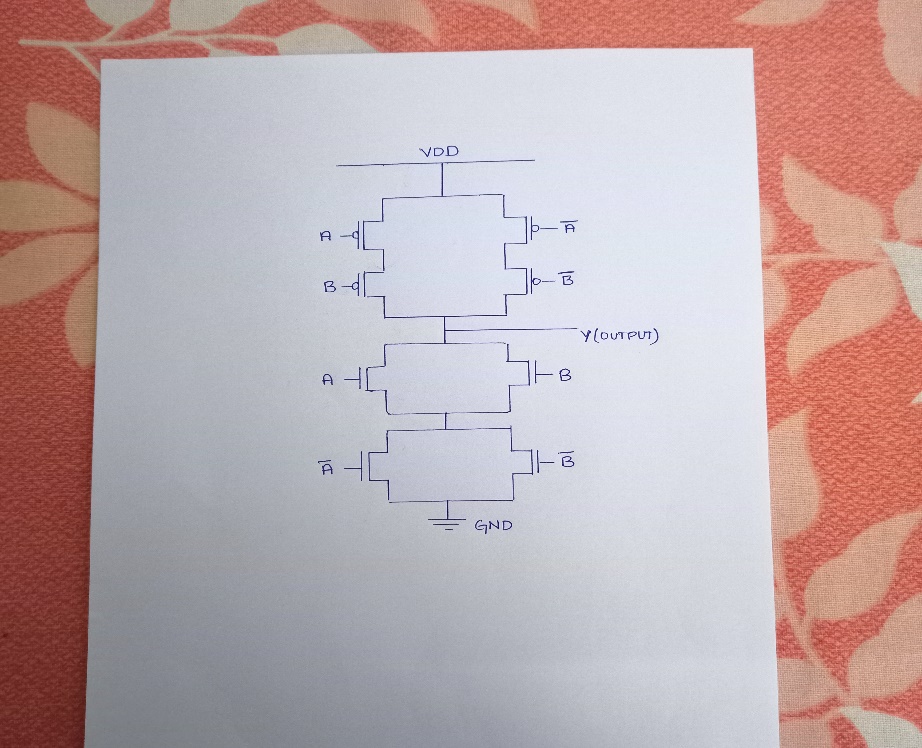


Figure 1 XNOR CMOS Circuit

# **Reference Circuit Waveform**

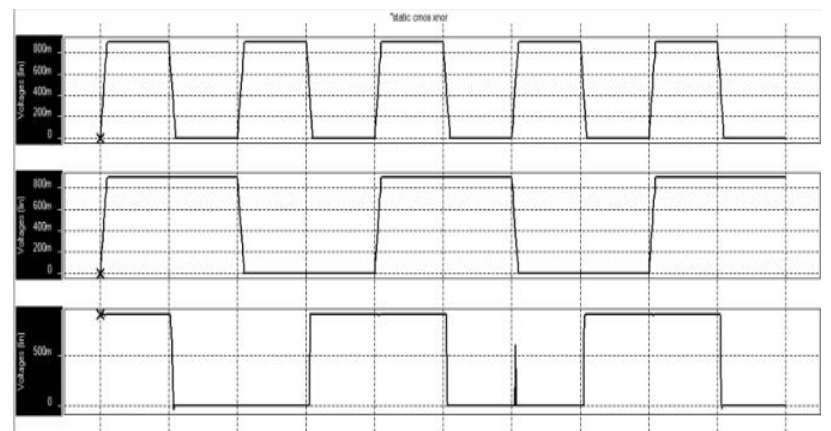


Figure 2 XNOR Circuit Waveform

This waveform is taken from reference 1.

##### **References**

1. Aditi Joshi, Chanchal Jain, Pooja Choudhary, Chirag Arora and Krishan Rapswal, “ A Comparative Performance Analysis of Various CMOS Design Techniques for XOR and XNOR Circuits”, International Journal for Research in Applied Science & Engineering Technology (IJRASET),ISSN: 2321-9653, Volume 5 Issue IV, April 2017.